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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,230	12/02/2003	Serge Francois Drogi	55123P265	5369

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EXAMINER	
VLAHOS, SOPHIA	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,230	DROGI ET AL.	
	Examiner	Art Unit	
	SOPHIA VLAHOS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *86-94* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *86-94* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 11/19/2007 have been fully considered but they are not persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., Applicant states: "Maligeorgos still couples a data clock between circuits, as is common in the prior art." citing column 22, lines 11-17 of U.S. 7,221,921) are not recited in the rejected claim(s). Although the claims are interpreted in light of the relevant the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

See that new claim 86, recites: "....for converting the baseband signal to a serial digital signal....for output, without a data rate clock signal, to a second integrated circuit;" broadly interpreted as not using a data rate clock signal in the transmission of the serial data signal (i.e. the serial data signal does not include an embedded clock signal ? or the serial data signal is generated without using a data rate clock?). Regardless, the limitation: "....for converting the baseband signal to a serial digital signal....for output, without a data rate clock signal, to a second integrated circuit;" (in itself is broad lacks clarity) is disclosed by Maligeorgos et. al., see Fig. 9A where the 910 is the first integrated circuit and blocks 905 and 120 (in an embodiment the baseband processor 120 assumes the functions of the Rx digital circuit 905) corresponding to the second integrated circuit. Received Data is sent from block 910 to

blocks 905 and 120, without a data rate clock signal (SCLK 950), since the SCLK is transmitted from the second integrated to circuit to the first (as shown in Fig. 11A).

Independent claims 91 and 94 also include "....for converting the baseband signal to a serial digital signal....for output, without a data rate clock signal, to a second integrated circuit;" and are rejected based on a similar rationale (see rejections below).

Information Disclosure Statement

2. In communication "Notice of Copending U.S. Patent Applications" received on 11/19/2007, a list of references is submitted "....under Information Disclosure Statement concurrently herewith." However, an "Information Disclosure Statement by Applicant" form listing the newly submitted references has not been received. The references listed in the "Notice of Copending U.S. Patent Applications" communication have not been considered.

Claim Objections

2. Claim 89 is objected to because of the following: claim 89 recites: "...is controlled by a data rate clock...." Since claim 89 depends on claim 86 that already mentions "a data rate clock" it should be clarified whether the "data rate clock" of claim is the same (or another data rate clock) as the data rate clock of claim 86.

Claim 90 is objected to because of the following: claim 90 recites: "...configured to convert digital data to be transmitted into a serial digital signal using a single bit delta modulator" since the single bit delta modulator is an A/D converter, the limitations is

interpreted as converting digital data using an 1-bit A/D converter to serial digital data, which does not make a lot of sense.

Claims 93 and 94 recite similar limitations as the one of claim 90 above and are also objected to for the same reason.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 86-88, 89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (U.S. 7,221,921) in view of Hill (U.S. 6,507,607).

With respect to claim 86, Maligeorgos et. al., disclose: a first integrated circuit for receiving an RF signal and converting the RF signal to a baseband signal (Fig. 2D , Rx analog circuitry 208, more details shown in Fig. 8, block 839, where the outputs of the down-converter 409, are baseband signals (I and Q), see column 10, lines 46-48, column 19, lines 5-10) and for converting the baseband signal to a serial digital signal using a one-bit sigma delta modulator (block 836, ADC circuit, column 19, lines 20-25, column 21, lines 48-51 sigma-deltaADC) for output , without a data rate clock signal, to a second integrated circuit (Fig. 2D and/or Fig. 8 see transmission of serial digital baseband signals from Rx Analog circuit to Rx Digital circuit (Fig. 9A see blocks 910 (Rx Analog circuit) and 905 (Rx Digital circuit) lines 960, 965 used for received data

transmission to Rx Digital circuit, and see that the SCLK the serial clock on line 950 is not output from the first IC to the second IC (but the other way around see Fig. 11A, clock signal is sent from Rx Digital to Rx Analog) and the second integrated circuit having a digital signal processor for receiving the serial digital signal output of the first integrated circuit (embodiment shown in Fig. 2D, and column 16, lines 23-26 where the functionalities of the Rx Digital circuit are assumed by the baseband processor (DSP see column 9, lines 35-39)), and recovering digital data in the received RF signal (see Fig. 11A, Rx digital side, the recovered digital data correspond to the realigned digital I and Q signals out of 1123A and 1123B that are supplied to other circuits in the baseband processor, and since the invention relates to cellular applications (see column 2, lines 56-58) it is understood that voice signals (as an example) are output from the reconstructed digital signals)

Maligoergos et. al., do not expressly teach: reconstructing the data rate clock (in this case clock signal 220 as shown in Fig. 2D).

In the same field of endeavor (RF communication) Hill teaches reconstructing a data rate clock (using a PLL to stabilize a clock signal, see column 5, lines 5-7)

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to modify the system of Maligoergos et. al., based on the teachings of Hill, to reconstruct (stabilize) the data rate clock , so that the data rate clock of Maligeorgos is stabilized (reconstructed) when received from reference generator circuitry and supplied to the signal processor circuitry 1110 of Fig 11A.

With respect to claim 87, see above rejection of claim 86.

With respect to claim 88, Maligeorgos et. al., disclose: wherein the I and Q digital signals are coupled from the fist integrated circuit to the second integrated circuit using low voltage differential coupling (see column 23, lines 45-55, use of low voltage swing differential signals).

5. Claims 89, 91-92, are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (7,221,921) in view of Hill (U.S. 6,507,607) and further in view of Khlat et. al., (U.S. 2004/0038652).

With respect to claim 89, neither Maligeorgos et. al.,nor Hill expressly teach: wherein the sigma delta modulator is controlled by a data rate clock, the data rate clock being programmable to provide various data rates in the serial digital signal for operation in various wireless communication systems.

In the same field of endeavor, Khlat et. al., disclose: wherein the sigma delta modulator is controlled by a data rate clock, the data rate clock being programmable to provide various data rates for operation in various wireless communication systems. (see Fig. 2, where the sigma-delta modulators have fs sampling frequencies, and block 199 generates the sampling frequencies for the different system modes (paragraph [0013] and see table 1 different sampling frequencies and paragraph [0022] where PLL generates the frequencies (clocks for the ADC)).

At the time of the invention, it would have been obvious to a person skilled in the art to modify the system of Maligeorgos et. al. and Behrens based on the teachings of Khlat et. al., so that sigma delta modulator is controlled by a data rate clock, the data rate clock being programmable to provide various data rates in the serial digital bit stream for various wireless communication systems and the motivation to perform such a modification is reception of signals of different standards (for example GSM clock frequency is 13MHz, see Maligeorgos et. al. column 11, lines 50-52 and Khlat et. al., Table 1, (sampling frequency) whereas other standards require different sampling clocks see table 1 of Khlat et. al.)).

6. Claim 90 is rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (7,221,921) in view of Hill (U.S. 6,507,607) and further in view of Sorrells et. al., (U.S. 2004/0013177).

With respect to claim 90, neither Maligeorgos et. al., nor Hill expressly teach: wherein the second integrated circuit is also configured to convert digital data to be

transmitted into a serial digital signal using a single bit sigma delta modulator for output, without a data rate clock signal, to the first integrated circuit, and the first integrated circuit is configured to receive the serial digital signal output of the first integrated circuit, to recover the digital data to be transmitted and modulate the digital data for RF transmission.

In the same field of endeavor, Sorrells et. al., discloses: wherein a second integrated circuit (Fig. 3A Baseband processor inside of 304 corresponds to a second integrated circuit , and block 202 corresponds to a first integrated circuit see paragraph [0052]) is also configured to convert digital data to be transmitted into a serial digital signal for output (paragraphs [0094][-[0095] where the baseband processor generates digital signals and uses serial bus to transmit the digital data), without a data rate clock signal (Fig. 5 and Fig. 6 block 110 of block 304 baseband processor shown in Fig. 6, signals out of 654, 652 (transmit filters see paragraph [0082]) on transmit side, see that reference clock 126d is received from the IC shown in Fig. 5 and is not output to it), and the first integrated circuit is configured to receive the serial digital signal output of the first integrated circuit (Fig. 3A, block 202), to recover the digital data to be transmitted and modulate the digital data for RF transmission (see Fig. 6 and Fig. 5 D/A conversion of signals to be transmitted 604b, 604c and processing shown in Fig. 5 to generate RF signals to be transmitted).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the system of Maligeorgos et. al., and Hill based on the teachings of Sorrells, so that the second integrated circuit is also configured to convert

digital data to be transmitted into a serial digital signal for output, without a data rate clock signal, to the first integrated circuit, and the first integrated circuit is configured to receive the serial digital signal output of the first integrated circuit, to recover the digital data to be transmitted and modulate the digital data for RF transmission to allow for increased integration and implementation of digital interfaces, and reduces costs (see last two sentences of paragraph [0075])

With respect to using a single bit sigma delta modulator to convert the digital data into a serial digital signal, Maligeorgos et. al., already teaches using single bit sigma delta modulators (column 15, lines 60-65, column 21, lines 50-52) and therefore it would have been obvious to a person of ordinary skill in the art to use sigma delta modulators to convert data received in block 304 (from a device see paragraph [0101]-[0102] cell phone, analog signals) into serial digital signal, using bit sigma delta modulators, since sigma-delta modulator are known in the art to perform accurate A/D conversion and using 1-bit requires less memory/storage in the system.

7. Claims 93 -94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maligeorgos et. al., (7,221,921) in view of Hill (U.S. 6,507,607), Khlat et. al., (U.S. 2004/0038652) and Sorrells et. al., (U.S. 2004/0013177).

With respect to claims 93- 94 these claims are rejected based on a rationale similar to the one used to reject claims 89 and 90 above.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SOPHIA VLAHOS whose telephone number is 571 272 5507. The examiner can normally be reached on MTWRF 8:30-17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SV
1/14/2008

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